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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,448	09/16/2003	Georg Muller	BGJ-102	1586

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EXAMINER	
CHAN, EMILY Y	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 09/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/663,448	MULLER, GEORG	
	Examiner	Art Unit	
	Emily Y. Chan	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 5-12* is/are rejected.

7)☒ Claim(s) *2-4* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 9 is objected to because of the following informalities: The recitation " that [redacted] setting is selected that is to be used during regular operation" is unclear since it is not specified what the "setting" [redacted] stands for. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 5 -12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rosefield et al US Patent No. 6,541,996 in view of Yoshizaki US patent No. 6,400,177.

With respect to claims 1, 8 and 10, Rosefield et al ('996) expressly disclose a method (see Figs 1-4) for measuring and trimming the impedance of driver devices (102, IMPEDANCE MEASUREMENT) during a test (see Fig. 2, pull up test EN and pull down test EN) being carried out before the regular operation of the semiconductor device (chip), the driver devices (102) of the semiconductor device including each a pull up circuit (204, pull up impedance matching array) and a pull down circuit (206, pull down impedance matching

array) (Col. 2, lines 54-65 "on-chip programmable pull up impedance matching array and pull down impedance matching array"), the method comprising :

joint activating of both the pull-up circuit (see Fig. 3, step 301 "enable pull up imped array) and the pull-down circuit (see Fig. 3, step 308 "enable pull down imped array), and

determining a total impedance of the pull up and pull down circuits (see Col. 9, lines 21-22 and 27-29).

Rosefield et al ('996) do not disclose the step of determining a first current flowing through the pull-up circuit or the pull-down circuit respectively.

Yoshizaki ('177) discloses an output driver (see Fig. 4) comprising pull up circuit (P1-4) and pull down circuit (N1-4). Yoshizaki ('177) exclusively teaches a method for meeting specified output impedance and current characteristics comprising the step of determining a first current flow (ILH, IHL) through a pull-down circuit (P1-4) or the pull down circuit (N1-4) (see Col. 4, lines 15-65).

Therefore, It would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to incorporate the step of determining the current flow through the pull up and/or pull-down circuit as taught by Yoshizaki ('177) into Rosefield et al ('996)'s method so that Rosefield et al ('996) 's method comprising the step of determination the current flowing through the pull up and the pull-down circuit for the expected benefit of having a transistor's impedance and current flow adjusted to better meet the requirement of particular applications as disclosed by because Yoshizaki ('177) (see Col. 3, lines 1-5).

With respect to claims 5-6, Yoshizaki ('177) discloses determining a voltage dropping over the pull-up and/or pull-down circuit, in particular with jointly activated pull-up and pull-down circuits (see Col. 4, lines 17-48).

With respect to claim 7, Yoshizaki ('177) discloses that the method steps are performed several times in sequence (see Fig. 3, step 314 "wait for restart"), each with different settings of transistors contained in the pull-up or pull down circuit (see Fig. 4 transistors contained in the pull up circuit (204) and in the pull down circuit (206)).

With respect to claim 9, Yoshizaki ('177) discloses that on the basis of the first current and voltage dropping over the pull up and pull down circuits as determined (see Col. 4, lines 17-48), the " setting" is elected (see Col. 3, line 16 " to set an impedance lever ") that is to be used during regular operation of the device.

With respect to claim 11, Rosefield et al ('996) discloses that a test device (comparator 209) is a test device not used for the driving of output signals during the regular operation of the semiconductor device and is for selecting the driver setting for at least one other semiconductor device (chip) during the test carried out before the regular operation of the at least one other semiconductor device (chip).

With respect to claim 12, Rosefield et al ('996) discloses that the test device (comparator 209) is connected with a device (208) provided on the semiconductor device (chip) itself, by means of which a voltage dropping over the pull-up and/or pull-down circuit is determined.

Allowable Subject Matter

3. Claims 2-4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

4. Claims 2-4 are indicated allowable because the prior art in the record does not teach or suggest the steps of joint de-activating both the pull-up circuit and the pull-down circuit; and determining a standby current flowing between the supply voltage pad and the ground connection with jointly de-activated pull-up and pull down circuits. Claims 3-4 are dependent on claim 2 and are indicated allowable accordingly.

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Savignac et al I US patent No. 6,693,447 disclose a device for testing semiconductor device (see Figs 2-4) comprising pull-up circuit and pull-down circuit.

Response to Arguments

6. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

Response to Amendment

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.**

See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emily Y. Chan whose telephone number is 571-272-1956. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SUPERVISORY PATENT EXAMINER
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EC
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